Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 21-37.

Listing of Claims:

1. (Original) A semiconductor structure, comprising:

a polycrystalline layer; and

a rough layer formed from an undoped silicon, the rough layer being formed on the polycrystalline layer and including protrusions extending from a surface of the layer.

2. (Original) The semiconductor structure of claim 1, wherein the protrusions include hemispherical protrusions.

3. (Original) The semiconductor structure of claim 1, wherein the polycrystalline layer comprises a conductive polycrystalline material.

4. (Original) The semiconductor structure of claim 1, wherein the polycrystalline layer comprises a conductive alloy that becomes polycrystalline at a temperature greater than about 500 degrees Celsius.

5. (Original) The semiconductor structure of claim 1, wherein the polycrystalline layer comprises a bottom electrode of a capacitor and wherein the protrusions of the rough layer increase the surface area of the bottom electrode so as to increase the capacitance of the capacitor.

6. (Original) A capacitor, comprising:

a top electrode;

a dielectric coupled to the top electrode; and

a bottom electrode coupled to the dielectric, wherein the bottom electrode includes a rough layer and an electrode layer, wherein the rough layer includes hemispherical

protrusions formed from undoped silicon, and wherein the electrode layer is formed from a polycrystalline material.

7. (Original) The capacitor of claim 6, wherein the electrode layer of the bottom electrode forms an outer surface of the capacitor, and wherein the rough layer forms an inner surface of the capacitor.

8. (Original) The capacitor of claim 6, wherein the bottom electrode comprises an outer surface, an embedded layer, and an inner surface to define a container structure, wherein the rough layer defines the inner surface and the outer surface, and wherein the relatively smooth surface defines the embedded layer.

9. (Original) The capacitor of claim 6, wherein the undoped silicon includes undoped amorphous silicon.

10. (Original) The capacitor of claim 6, wherein the electrode layer is a polycrystalline alloy selected from a combination of silicon and germanium.

11. (Original) A semiconductor structure, comprising:

a first capacitor having a bottom electrode having an outer surface and an inner surface, wherein the outer surface of the bottom electrode of the first capacitor is smooth, and wherein the inner surface of the bottom electrode of the first capacitor is rough from a number of hemispherical protrusions; and

a second capacitor having a bottom electrode having an outer surface and an inner surface, wherein the outer surface of the bottom electrode of the second capacitor is smooth and is near the outer surface of the bottom electrode of the first capacitor such that the first and the second capacitor exists in close proximity without shorting, and wherein the inner surface of the bottom electrode of the second capacitor is rough from a number of hemispherical protrusions.

12. (Original) The semiconductor structure of claim 11, wherein a portion of the outer surface of the bottom electrode of the first capacitor is housed in a nonconductive

material so as to expose the rest of the outer surface of the bottom electrode of the first capacitor, and wherein a portion of the outer surface of the bottom electrode of the second capacitor is housed in the nonconductive material so as to expose the rest of the outer surface of the bottom electrode of the second capacitor.

13. (Original) The semiconductor structure of claim 11, wherein the outer surfaces of the bottom electrodes of the first and second capacitors are composed of a material selected from undoped silicon.

14. (Original) The semiconductor structure of claim 11, wherein the inner surfaces of the bottom electrodes of the first and second capacitors are composed of a material selected from polycrystalline silicon-germanium.

15. (Original) The semiconductor structure of claim 11, wherein the first capacitor includes a first dielectric layer that overlies the bottom electrode of the first capacitor and a first top electrode that overlies the first dielectric layer, and wherein the second capacitor includes a second dielectric layer that overlies the bottom electrode of the second capacitor and a second top electrode that overlies the second dielectric layer.

16. (Original) A method for making a semiconductor structure, comprising:

forming a polycrystalline layer ; and

forming hemispherical protrusions in an undoped silicon layer that overlies the polycrystalline layer.

17. (Original) The method of claim 16, wherein forming a polycrystalline layer includes forming a silicon-germanium alloy.

18. (Original) The method of claim 16, wherein forming hemispherical protrusions includes depositing the undoped silicon layer by using low-pressure chemical vapor deposition of silane gas at a temperature less than about 550 degrees Celsius and greater than about 450 degrees Celsius.

19. (Original) The method of claim 18, wherein forming hemispherical protrusions includes forming atomic seeds from which hemispherical protrusions are grown by chemical vapor deposition of silane gas at a temperature less than about 600 degrees Celsius and greater than about 550 degrees Celsius.

20. (Original) The method of claim 19, wherein forming hemispherical protrusions includes annealing so as to grow the atomic seeds to form hemispherical protrusions.

21-37. (Cancelled)

38. (Original) A semiconductor structure, comprising:

a first layer formed from an undoped substance and including first and second surfaces, the first surface including a plurality of surface protrusions that increase a surface area of the first layer; and

a second layer formed abutting the second surface of the first layer and including a plurality of atoms, the atoms in the second layer being sufficiently bound in the second layer to substantially remain in the second layer during formation of the first layer.

39. (Original) The semiconductor structure of claim 38, wherein the first layer comprises an undoped silicon layer.

40. (Original) The semiconductor structure of claim 38 wherein the undoped silicon layer comprises an undoped amorphous silicon layer.

41. (Original) The semiconductor structure of claim 38 wherein the second layer comprises a polycrystalline layer.

42. (Original) A capacitor, comprising:

a first electrode layer having first and second surfaces formed from undoped silicon;

first and second rough layers formed on the first and second surfaces of the first electrode layer, respectively, each of the first and second rough layers including a plurality of surface protrusions that increase a corresponding surface area of the layer;

a dielectric layer formed on the first and second HSG layers; and

a second electrode layer formed on the dielectric layer.

43. (Original) The capacitor of claim 42, wherein the first electrode layer comprises a polycrystalline layer.

44. (Original) The capacitor of claim 42, wherein the first and second rough layers comprise first and second HSG layers, respectively.

45. (Original) The capacitor of claim 42, wherein the first rough layer is formed over substantially the entire first surface of the first electrode layer and wherein the second rough layer comprises a segment formed on a first portion of the second surface of the first electrode layer and another segment formed on a second portion of the second surface of the first electrode layer.

46. (Original) The capacitor of claim 43, wherein the first electrode layer comprises a U-shaped structure and the first surface corresponds to an inner surface and the second surface corresponds to an outer surface.

47. (Original) A capacitor, comprising:

a first electrode layer having first and second surfaces formed from undoped silicon;

a rough layer formed on the first surface of the first electrode layer, the rough layer including a plurality of surface protrusions that increase a corresponding surface area of the layer;

a dielectric layer formed on the rough layer and on the second surface of the first electrode layer; and

a second electrode layer formed on the dielectric layer.

48. (Original) The capacitor of claim 47, wherein the first electrode layer comprises a polycrystalline layer.

49. (Original) The capacitor of claim 47, wherein the first and second rough layers comprise first and second HSG layers, respectively.

50. (Original) The capacitor of claim 47, wherein the dielectric layer comprises a first segment formed on a first portion of the second surface of the first electrode layer and a second segment formed on a second portion of the second surface of the first electrode layer.

51. (Original) The capacitor of claim 47, wherein the first electrode layer comprises a U-shaped structure and the first surface corresponds to an inner surface and the second surface corresponds to an outer surface.